REMARKS

Regarding objections to the claims:

Claims 3-6 are objected to because of the following informalities: Claim 3 recites the limitation "the conductive element" and "the inductor" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Response:

Claim 3 is duly amended to read "a conductive element" and "an inductor" in line 2. Claims 4-6, being dependent upon claim 3, should be allowed if the amended claim 3 is considered allowable. Reconsideration of amended claim 3 and dependent claims 4-6 is politely requested.

Regarding objections to the drawings:

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, a first conductive trace formed on the top wiring layer (the first wiring layer), as recited in claim 1, and conductive traces disposed on separate wiring layers, as recited in claim 3, must be shown or the feature(s) canceled from the claim(s).

Response:

The Applicant points out that the amended Fig.3 of the present invention, clearly depicts a conductive trace (24), shown by an emboldened line, on a first wiring layer (16). It should be understood that Fig.3 is a three dimensional representation, having axes X, Y and Z as indicated; the spatial relationships between the various conductive traces and vias being shown in solid, and the printed circuit board layers shown in phantom, since, for example, these layers may occur within the bulk of the circuit board. The plane 16 of Fig.3 represents the first wiring layer upon which a first conductive trace is formed (item 24 is an example of such a trace), and the plane 18 represents a second wiring layer upon which a second conductive trace (e.g. item 26) is formed. These features correspond with the indexed description of the Detailed Description of the instant application (paragraph 0016), and can also further be set in context by reference to Fig.4 (paragraph 0017 refers), which shows the same two layers (16 and 18) and a conductive trace (24) in cross-section, as part of a multi-layer printed circuit board (34).

Therefore, the Applicant asserts that the drawings, in particular amended Fig.3, show both "a first conductive trace (20) formed on a first wiring layer (16) of a printed circuit board (34)", and "a plurality of conductive traces (20 and 22) formed on a plurality of wiring layers (16 and 18) of a printed circuit board (34)".

In light of the argument set forth above, reconsideration of the drawings is politely requested. If, on the other hand, the Examiner maintains this objection, the Applicant respectfully requests that the Examiner be more specific.

Regarding claim rejections under 35 USC 112:

Claims 1-6 are rejected under 35 USC 112, first paragraph, as failing to comply with the written description requirement...There is no support in the disclosure for a first conductive trace formed on the top wiring layer (the first wiring layer), as recited in claim 1, and there is also no support for conductive traces disposed on separate wiring layers, as recited in claim 3.

Response:

The Applicant politely refers the Examiner to the above argument directed at objections to the drawings, as the Applicant feels that the key points of said argument are closely related to the above cited rejections. Therefore the Applicant repeats the assertion that the drawings show both "a first conductive trace (20) formed on a first wiring layer (16) of a printed circuit board (34)", and "a plurality of conductive traces (20 and 22) formed on a plurality of wiring layers (16 and 18) of a printed circuit board (34)", and moreover that the drawings, in concert with the indexed description of the specification, particularly paragraphs [0016] and [0017], in no way suggest that "**Figure 3 depicts a first** (20) **and a second** (22) **conductive traces formed between the first** (16) **and second** (18) **wiring layers**".

Reconsideration of claims 1 and 3 in light of the arguments set forth above, is politely requested. Claims 2 and 4-6, being dependent upon claims 1 and 3 respectively, should be allowed if claims 1 and 3 are considered allowable.

Claims 1-6 are rejected under 35 USC 112, first paragraph, as failing to comply with the written description requirement. There is no support for a conductive trace having at least an end disposed coincident with an end of a conductive trace disposed on a separate layer, as recited in claim 3.

Response:

Paragraph 0016 of the Detailed Description of the instant application clearly and unambiguously establishes the following: that the first wiring layer (16) and second wiring layer (18) are parallel, that a first conductive trace (20) is formed on the first wiring layer (16), that a second conductive trace (22) formed on the second wiring layer (18), that a first via plug (28) is perpendicular to the first conductive trace (20) (and thereby perpendicular to the second conductive trace (22) as the layers upon which the respective traces are formed are parallel), and that an end of first conductive trace (20) and an end of the second conductive trace (22) are connected to the first via plug (28). For this to be true, an end of the first trace (20) would have to (by the principles of geometry) coincide with an end of the second trace (22), the second trace being disposed on a separate layer (the second wiring layer 18, as stated above). Hence, there is clear support for a conductive trace having at least an end disposed coincident with an end of a conductive trace disposed on a separate layer, as recited in claim 3. The structure as recited is, the Applicant believes, unambiguously depicted in the amended figures, Fig.3 and Fig.4.

Reconsideration of claims 1 and 3 in light of the argument set forth above, is politely requested. Claims 2 and 4-6, being dependent upon claims 1 and 3 respectively, should be allowed if claims 1 and 3 are considered allowable.

Claims 1-6 are rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Response:

Wiring layers are exceedingly well known in the art of printed circuit boards. The Applicant contends that one of ordinary skill in this art, upon reading the claims, would know the structural relationship of the wiring layers and the printed circuit board recited in amended claims 1 and 3. Specifically, multi-layered printed circuit boards and the concept of disposing traces on both sides of a single-layered board are elementary in this art. In view of this, the Applicant argues that reciting additional limitations as to the specific stacking arrangements of the wiring layers would unfairly limit the scope of the claims.

Regarding the limitations of claim 3 wherein the ends of conductive traces are coincident, please see the response in the above section. In addition, the term coincident typically means to "occupy the same space", however, the number of dimensions of such space (i.e. 2-D or 3-D) is not part of such definition. The layers recited unequivocally make three-dimensional coincidence impossible, and this was actually intended in drafting the claim. Thus, "occupying the same space in two dimensions" is the only meaningful interpretation of the term coincident. Moreover, since, one of ordinary skill in this art is well aware of the layered circuit board concept, such individual would naturally read coincident as meaning "occupying the same space in two dimensions" or "apparently coincident from one view point". Furthermore, preliminary redrafts of claim 3 that did not contain the word "coincident", were found to be either too wordy to be clearly understood, or were found to be unfairly limiting the claimed invention.

Reconsideration of this rejection in view of the above arguments is respectfully requested.

Regarding claim rejections under 35 USC 103:

Claims 1-6, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Liou (6,037,649) in view of Gardner (6,452,247).

Response:

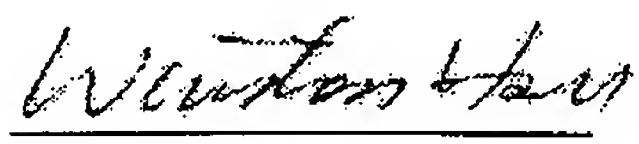
In an effort to overcome the above cited rejections under 35 U.S.C. 103(a), claims 1 and 3 are amended by the addition of further limitations that better reflect the nature of the present invention, and new claims 7 and 8 are added to reflect further embodiments, particularly those depicted in Figs.7 and 8, whereby the present invention method of implementing inductances on printed circuit board substrate, allows higher degrees of flexibility than do the cited arts.

In both the teachings of Liou and Gardner, all vias (or equivalent structures) are arranged along significantly parallel lines, thus reducing flexibility. Whereas the present invention overcomes the rigid requirements on space usage inherent in the prior arts, by allowing increased flexibility in printed circuit board design. As neither Liou nor Gardner teaches forming inductors in such a way, i.e. not arranged upon significantly parallel lines, the present invention could therefore not be realized by a combination of their teachings without

further inventive process.

Reconsideration of amended claims 1 and 3, claims 2 and 7 (being dependent upon claim 1) and claims 4-6 and 8 (being dependent upon claim 3), is politely requested. No new matter is introduced by the above amendments.

Sincerely yours,



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